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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kiran Ganesh et al.

Title: 2-DIMENSIONAL PLACEMENT WITH RELIABILITY CONSTRAINTS FOR VLSI DESIGN

Docket No.: 884.141US1

Serial No.: 09/431,477

Filed: November 1, 1999

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Examiner: Phallaka Kik

Group Art Unit: 2825

Commissioner for Patents
Washington, D.C. 20231

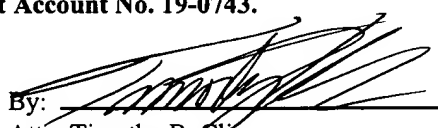
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We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ A return postcard.
- ☒ An Amendment and Response Under 37 CFR 1.111 (8 Pages).
- ☒ Petition for Extension of Time (1 pg.)
- ☒ A check in the amount of \$920.00 to cover the Extension of Time Fee.
- ☒ Clean Version of Pending Claims (5 pgs.).

Please consider this a **PETITION FOR EXTENSION OF TIME** for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

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By: 
Atty: Timothy B. Chase
Reg. No. 40,987

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 26 day of March, 2002.

Jane E. Brockschink
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